



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|----------------------------------|------------------|
| 10/676,483 | 09/30/2003 | Andrew J. Ogle | INSG0011 | 7523 |
| 7590 11/23/2005 | | | | |
| Paul Livesay, Smyrski & Livesay, LLP 751 Laurel Street, #438 San Carlos, CA 94070 | | | EXAMINER KROFCHECK, MICHAEL C | |
| | | | ART UNIT 2186 | PAPER NUMBER |

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|--------------------------------------|--|--|
| Office Action Summary | Application No. 10/676,483 | Applicant(s) OGLE, ANDREW J. | |
| | Examiner Michael Krofcheck | Art Unit 2186 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6, 8-11 and 13-18 is/are rejected.
- 7) ☒ Claim(s) 1-8, 10-14 and 16-18 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to application 10/676,483 filed on 9/30/2003.
2. Claims 1-18 have been submitted for examination.
3. Claims 1-18 have been examined.

Specification

4. The disclosure is objected to because of the following informalities:
 - a. Line 15 of page 15 contains the unfinished thought of, "(see discussion of _____ below)*****."

Appropriate correction is required.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim. A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Art Unit: 2186

7. Claims 1-8, 10-14, 16 are objected to because of the following informalities:

- a. With respect to claim 1, the “a” at the end of line 16 should be removed.
- b. With respect to claims 5-8, the claims are improperly numbered. Claim 5 separates claims 6-8 from claim 3 and claim 7 separates claim 8 from claim 6.
- c. With respect to claim 10, the applicant neglected to state which claim, claim 10 depends from. The examiner assumes the applicant intended the claim to depend on claim 9.
- d. With respect to claim 11, the application states that it should depend on claim 8, which causes the claim to be separated by independent claim 9 and dependent claim 10 from its parent claim. It is the examiner’s interpretation that claim 11 was intended to depend on claim 9.
- e. With respect to claims 12 and 13, claim 12 separates claim 13 from its parent claim.
- f. With respect to claim 14, the examiner believes that the word “by” should be included between the words “value” and “a” in part b of the claim.
- g. With respect to claim 12 and 16, the 1st and 2nd status bits are opposite from the 1st and 2nd status bits mentioned in the spec and figure 9.
- h. Claims 2-4 are objected to because of their dependencies.

The applicant is reminded that in correcting the claim numbering to ensure that the claim dependencies are also correct. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 8, 13 and 15-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 8 recites the limitations "the copy-offset value" in line 2. There is insufficient antecedent basis for this limitation in the claim. It appears that the applicant may have intended claim 8 to be dependent on claim 7.

11. Claim 13 recites the limitations "the second status identifier", "such second status identifier", "the first status identifier", "said first status identifier", and "step (d) above" in the claim. There is insufficient antecedent basis for these limitations in the claim. It appears that the applicant may have intended claim 13 to be dependent on claim 12.

12. Claim 15 is indefinite and confusing as it contains grammatical and idiomatic errors in lines 20-22. The applicant states, "wherein one X of k to updated as instructed by the instruction set contained in the update package." It is the examiner interpretation that the applicant intended to state, wherein one block, X, of the k blocks to be updated as instructed by the instruction set contained in the update package

13. Claims 16-18 are rejected because of their dependencies.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

15. Claims 1-4, 9-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Kulkarni et al. U.S. Patent 6,775,423 (hereinafter Kulkarni).

16. With respect to claim 1, Kulkarni teaches of an updating system for transforming a first data image into a second data image, wherein said first image resides across k memory blocks of a block-structured non-volatile memory device contained in a client device (fig. 1; column 5, lines 12-32), said updating system comprising: a. An update generator (fig. 1; items 102; column 4, lines 11-50) that produces an update package resulting from a comparison between the first data image and the second data image (fig. 1; items 120 and 124; column 4, lines 28-50; where the differences file and modified differences file (update packages) is created by including the new data section from the new image and references to the old image for the repeated data)

whereby said comparison selects and encodes an instruction set comprising a plurality of SETBLOCK, COPY and ADD operations for each of the k memory blocks (figs. 2; column 5, lines 51-59; column 9, lines 42-58; where the modified differences file contains data sections that contain data from the new image (ADD operations) and copy sections (COPY operations). The header between each section gives specific information about the section following the header. The header thus separates the

different data sections (blocks) in the modified differences file indicating the order that the data sections are to be processed (SETBLOCK operations)); and

b. An update decoder resident on the client device whereby said update decoder interprets the instruction set of the update package and applies the update a package to update the k memory blocks (fig. 1; column 5, lines 20-25; where the flash manager (update decoder) is configured to collect data sections for the image to create the new image).

17. With respect to claim 2, Kulkarni teaches of all the limitations of the parent claim as discussed supra. Kulkarni also teaches of a communications network (fig. 1; column 4, lines 11-20; where the server includes a network interface for communicating with remote computing devices over a network, such as the Internet) and a host server (fig. 1; item 102) that comprises the update generator, whereby the update package is delivered from the host server to the client device via the communications network (fig. 6; column 9, lines 59-65; where the PDA (client device) dials into the server via the Internet and downloads the modified differences file).

18. With respect to claim 3, Kulkarni teaches of all the limitations of the parent claim as discussed supra. Kulkarni also teaches of wherein for each memory block X of k blocks an updated version of such Xth memory block is first constructed in a scratch memory (column 9, line 66-column 10, line 15; where the flash manager starts to build the new image and temporarily stores portions of it in the new memory block (scratch memory)), and

then memory block X is reprogrammed with the contents of the scratch memory (column 9, line 66-column 10, line 15; where the contents of the new memory block are written to the flash memory when the portion of the new image is greater than one-half the size of a write block in the flash memory).

19. With respect to claim 4, Kulkarni teaches of all the limitations of the parent claim as discussed supra. Kulkarni also teaches of wherein said k memory blocks are updated in a non-sequential order as specified by the SETBLOCK operations comprising the instruction set (figs. 2, 6; column 9, lines 42-58, column 9, line 66-column 10, line 1; where the modified differences file contains re-ordered sections that start with their respective headers. The order shown by the headers is the order the sections will be updated. As shown in the figure, the order is not sequential. The flash manager uses the modified differences file to build the new image).

20. With respect to claim 9, Kulkarni teaches of a method of updating to a second image a first image stored across k memory blocks of a non-volatile memory device contained in a client device (fig. 1; column 5, lines 12-32), said updating method comprising: a. Generating an update package by comparing the first image and the second image (fig. 1; items 120 and 124; column 4, lines 28-50; where the differences file and modified differences file (update packages) is created by including the new data section from the new image and references to the old image for the repeated data) and

using result of said comparison to encode an instruction set comprised of a plurality of SETBLOCK, COPY and ADD operations for each of the k memory blocks (figs. 2; column 5, lines 51-59; column 9, lines 42-58; where the modified differences file

contains data sections that contain data from the new image (ADD operations) and copy sections (COPY operations). The header between each section gives specific information about the section following the header. The header thus separates the different data sections (blocks) in the modified differences file indicating the order that the data sections are to be processed (SETBLOCK operations));

b. Applying the instruction set by interpreting the instruction set to direct the updating of the memory blocks in an order specified by the SETBLOCK operations (figs. 2, 6; column 9, lines 42-58, column 9, line 66-column 10, line 1; where the modified differences file contains re-ordered sections that start with their respective headers. The order shown by the headers is the order the sections will be updated. The flash manager uses the modified differences file to build the new image).

21. With respect to claim 10, Kulkarni teaches of all the limitations of the parent claim as discussed supra. Kulkarni also teaches of wherein said applying step further comprises, for each memory block X of k blocks, a. constructing an updated version of such Xth memory block in a scratch memory location accessible to the client device (column 9, line 66-column 10, line 15; where the flash manager starts to build the new image and temporarily stores portions of it in the new memory block (scratch memory)),

wherein said scratch memory location being at least as large as the largest of the k memory blocks (column 2, lines 42-63; where each RAM memory block corresponds to one flash memory block; The new memory block (scratch memory) a part of the RAM, therefore it is also the same size as the flash memory block (k memory block)), and

b. reprogramming Xth memory block with the contents of the scratch memory (column 9, line 66-column 10, line 15; where the contents of the new memory block are written to the flash memory when the portion of the new image is greater than one-half the size of a write block in the flash memory).

22. With respect to claim 11, Kulkarni teaches of all the limitations of the parent claim as discussed supra. Kulkarni also teaches of wherein the step of applying instruction set in an order specified by the SETBLOCK operation is a non-sequential order (figs. 2, 6; column 9, lines 42-58, column 9, line 66-column 10, line 1; where the modified differences file contains re-ordered sections that start with their respective headers. The order shown by the headers is the order the sections will be updated. As shown in the figure, the order is not sequential. The flash manager uses the modified differences file to build the new image).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

24. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

Art Unit: 2186

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

25. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kulkarni, and Estakhri et al., U.S. Patent 5,485,595 (hereinafter Estakhri).

26. With respect to claim 15, Kulkarni teaches of a system for reliably updating on a client device a first image stored across a plurality of memory blocks of a non-volatile memory device to create a second image, said system comprising: a. an update package including an instruction set (figs. 2; column 5, lines 51-59; where the differences file (update package) contains data sections, copy sections and headers between the sections that give specific information about the following section),

which instruction set comprises a plurality of ADD and COPY operations associated with each of the plurality of memory blocks to be updated (figs. 2; column 5, lines 51-59; where the differences file (update package) contains data sections (ADD operations), copy sections (COPY operations) and headers between the sections that give specific information about the following section);

wherein one X of k to updated as instructed by the instruction set contained in the update package (figs. 2; column 6, lines 1-34; where the differences file is set to modify the second block of the old image which contains 'def' to contain 'xyz');

c. an update decoder resident on said client device that interprets the update package and applies the instruction set to update the plurality of blocks on a block-by-block basis (fig. 1; column 5, lines 20-25; where the flash manager (update decoder) is configured to collect data sections for the image to create the new image), and

Kulkarni fails to explicitly teach of (1) a status array comprised of a least two switchable status identifiers associated with each of the plurality of memory blocks, (2) which update decoder accesses and manipulates the status identifiers when applying said instruction set.

However, Estakhri teaches of a status array comprised of a least two switchable status identifiers associated with each of the plurality of memory blocks (fig. 1; column 5, lines 4-8; where an old/new flag, used/free flag, and others are associated with each memory location (memory block)),

which update decoder accesses and manipulates the status identifiers when applying said instruction set (fig. 9; column 7, lines 1-25; where in writing to the flash memory, the system is unable to locate a block that has an unset used/free flag and subsequently erases the flags for all blocks with a set old/new flag).

Kulkarni, and Estakhri are analogous arts as they are both in the same field of endeavor, flash memory. It would have been obvious to one of ordinary skill in the art having the teachings of Kulkarni, and Estakhri at the time of the invention to incorporate the process of avoiding erasure cycles as taught in Estakhri into the flash memory in Kulkarni. The motivation for this would have been to lengthen the life of the flash memory by lessening the number of erasure cycles performed during use (Estakhri column 1, lines 34-43 & column 2, lines 60-61).

27. Claim 6, 8, 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kulkarni and Miller U.S. Patent 5,832,520 (hereinafter Miller).

Art Unit: 2186

28. With respect to claim 6, Kulkarni teaches of all the limitations of the parent claim as discussed supra. Kulkarni fails to explicitly teach of wherein the instruction set further comprises a plurality of COPYADD operations in lieu of at least a portion of the plurality of COPY operations.

However, Miller teaches of wherein the instruction set further comprises a plurality of COPYADD operations in lieu of at least a portion of the plurality of COPY operations (column 8, line 66-column 9, line 5; where an insert followed by a copy is returned as a raw DIFF command sequence. The order of the operation (insert or copy first) is arbitrary as one of ordinary skill in the art would have known that a list of individual insert and copy operations can be grouped into insert/copy or copy/insert operations and still achieve the same result).

Kulkarni and Miller are analogous arts as they are both in the same field of endeavor, using difference files to update data. It would have been obvious to one of ordinary skill in the art having the teachings of Kulkarni and Miller at the time of the invention to combine the data and copy sections of Kulkarni as is taught in Miller. The motivation for this would have been to decrease the size of the difference file (Miller, column 8, lines 57-65).

29. With respect to claim 8, the combination of Kulkarni and Miller teach of all the limitations of the parent claims as discussed supra. Kulkarni fails to explicitly teach of said update decoder further comprises a mode mechanism that switches the update decoder from using the copy-offset value to using a zero offset.

However, Miller teaches of said update decoder further comprises a mode mechanism that switches the update decoder from using the copy-offset value to using a zero offset (fig. 9, column 16, lines 41-64; where a copy move position command is executed which uses a new copy absolute offset; and a copy from current position command uses no offset (an offset of zero) and copies to the current position. The use of the different commands switches the command state machine from using or not using an offset).

Kulkarni and Miller are analogous arts as they are both in the same field of endeavor, using difference files to update data. It would have been obvious to one of ordinary skill in the art having the teachings of Kulkarni and Miller at the time of the invention to include a copy with a move to a new location and a copy to the same location operation in Kulkarni as is taught in Miller. The motivation for this would have been to decrease the size of the difference file as offset values would not be required for all operations (Miller, column 8, lines 57-65).

33. With respect to claim 14, Kulkarni teaches of all the limitations of the parent claim as discussed supra. Kulkarni fails to explicitly teach of maintaining a first copy-offset value and a second copy-offset value, and selection setting a copy-offset value a plurality of COPYOFFSET values in the client.

However, Miller teaches of maintaining a first copy-offset value and a second copy-offset value (fig. 9; column 16, lines 54-64; where within the difference file, there are multiple commands and each CMP command contains its own offset value), and

selection setting a copy-offset value a plurality of COPYOFFSET values in the client (fig. 9; column 16, lines 54-64; where within the difference file, there are multiple commands and each CMP command contains its own offset value. The offset value in each command is used as the offset value for that operation).

Kulkarni and Miller are analogous arts as they are both in the same field of endeavor, using difference files to update data. It would have been obvious to one of ordinary skill in the art having the teachings of Kulkarni and Miller at the time of the invention to include a copy with a move to a new location (offset) in Kulkarni as is taught in Miller. The motivation for this would have been to decrease the size of the difference file (Miller, column 8, lines 57-65).

Allowable Subject Matter

30. Claims 5, 7, 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

31. Claim 13, 16-18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

32. The following is a statement of reasons for the indication of allowable subject matter:

- a. With respect to claim 12, the prior art of Kulkarni teaches of Constructing an updated version of each Xth memory block in a scratch memory location

accessible to the client device wherein said scratch memory location is at least as large as the largest of the k memory blocks (as previously cited), and

Joshi (U.S Patent 5,414,839) teaches of b. Reprogramming a temporary memory block in a nonvolatile memory device with the contents of the scratch memory; d. Reprogramming the Xth memory block with the contents of the temporary memory block; and e. Switching a first switchable status identifier when step d is completed with respect to each memory block and switching a status identifier when step b is completed with respect to each memory block (column 6, lines 45-58).

The prior art fails to teach of Switching a **second** switchable status identifier when step b is completed with respect to each memory block as is taught in the claim.

b. With respect to claim 13, the prior art fails to teach of Checking the second status identifier for each Xth block; Then for the first block encountered for which such second status identifier is still set, checking the first status identifier with respect to such; and Proceeding to update such block commencing from step (d) above if said first status identifier is clear, or proceeding to update the subsequent block X+1 commencing at step (a) above as is taught in the claim.

c. With respect to claim 16, the prior art teaches of a status array of a first switchable status identifier associated with each Xth memory block of k to be updated, whereby the first switchable status identifier is switched from a first state to a second state when the updated code is reprogrammed into the Xth

memory block from said temporary memory device rather than with the contents of the scratch memory [status bit], Joshi column 6, lines 45-58.

The prior art fails to teach of whereby the second switchable status identifier is switched from a first state to a second state when the contents of the scratch memory are stored in a temporary memory block in a non-volatile memory device prior to said contents being reprogrammed into the Xth memory block as is taught in the claim.

d. With respect to claim 17, the prior art (Estakhri) teaches of the status array in the flash memory and fails to teach of wherein said status array is comprised in the update package as is taught in the claim.

e. With respect to claim 5, the prior art fails to teach of said update package further includes a status array comprised of at least two switchable status identifiers associated with each memory block X of k to be updated as instructed by the instruction set contained in the update package.

f. With respect to claim 7, the prior art of Miller teaches of using copy offset values in copying old data to the new image as cited above. The prior art does not teach of wherein said **update decoder** maintains **at least two** copy-offset values comprised of a current offset value and a non-current offset value, and wherein the instruction set of said update package further comprises a plurality of SETCOPYOFFSET operations, which SETCOPYOFFSET instructions are instruct the update decoder to toggle the copy-offset value between the current value and the non-current value.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Michael Krofcheck



MATTHEW D. ANDERSON
PRIMARY EXAMINER